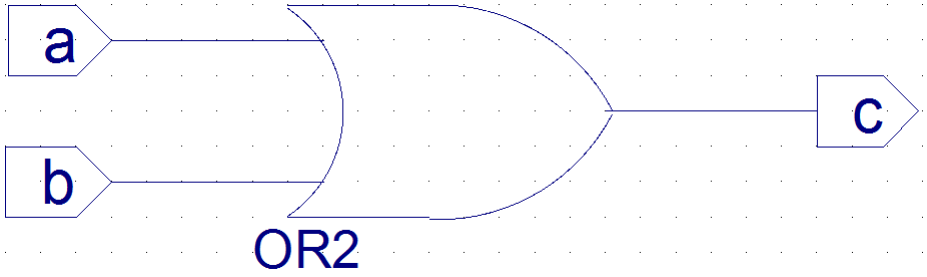
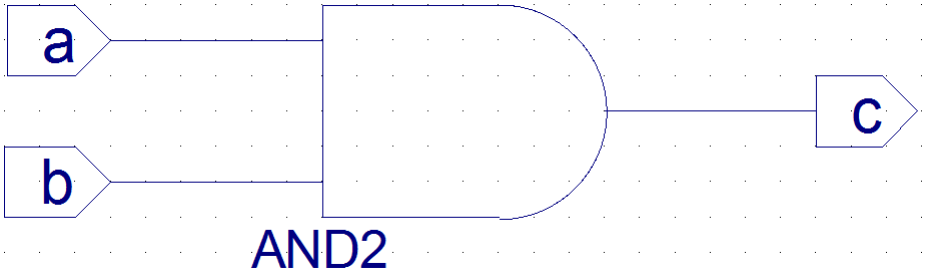
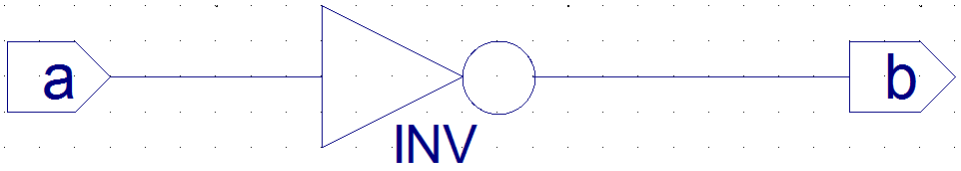
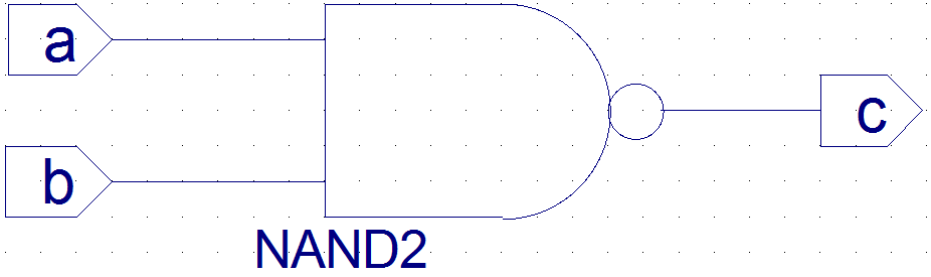
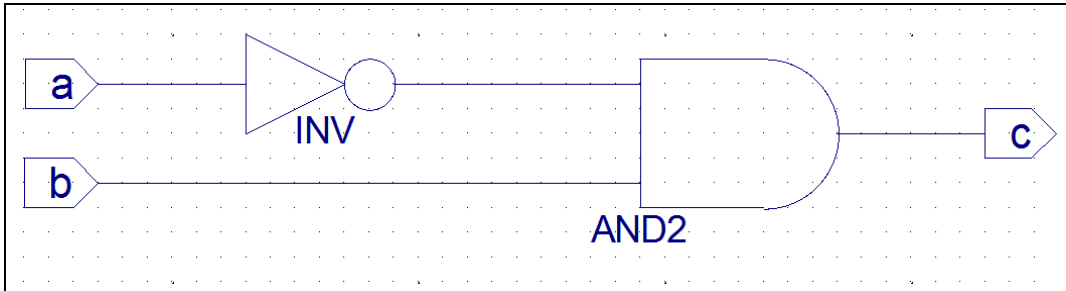
Schematic	Structural Verilog	Behavioral Verilog
	**or OR_GATE(c, a, b);**	**assign c = a | b;**
	**and I_GATE(c, a, b);**	**assign c = a & b;**
	**not NOT_GATE(b, a);**	**assign b = ~a;**
	**nand NAND_GATE(c, a, b);**	**assign c = ~(a & b);**

	**not NOT1(not_wire, a);** **and AND1(c, not_wire, b);**	**assign c = (~a) & (b);**