PWM Reference Component

DIGILENT RO

Overview

This document describes the VHDL implementation of a PWM (pulse width modulation) wave generator. The PWM wave generator reference component file is PWM.vhd.

This reference component generates a PWM wave using a clock input signal and an 8-bit reference value which determines the width of the pulse.

Functional Description

A PWM signal can be generated using a counter that increments periodically (it is connected to the clock on the board) and that resets at the end of every period of the PWM signal. When the counter value is more than the reference value, the PWM output changes state from high to low (or low to high).

The PWM module generates the PWM signal using the clock input and an 8-bit input *cmpPwm*. *CmpPwm* is a reference value which is compared with the internal counter value. When *cmpPwm* = 0 the pulse width is minimum (output LOW), and when *cmpPwm* = 255 the pulse width is maximum (output HIGH). The pulse width is proportional to the reference value.
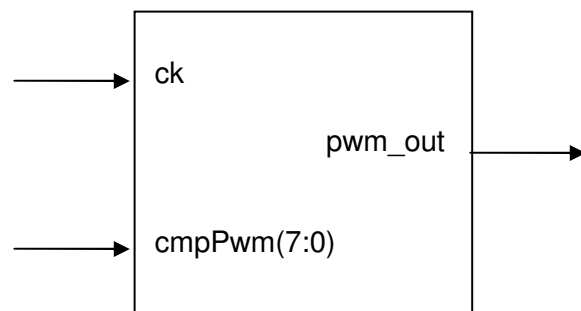

Figure 1 *The PWM Reference Component*

For generating the output signal an 8-bit counter (*cntPwm*) is used. When the value of the counter (*cntPwm*) is less than the reference value (*cmpPwm*), the output signal (*pwmOut*) is HIGH, and when the value of the counter (*cntPwm*) is greater than or equal to the reference value of *cmpPwm*, the output signal (*pwmOut*) is LOW. The *CntPwm* is an 8-bit value which is part of a bigger counter, the counter is 8 + *ckPwmRange* bits long. The frequency of this counter is equal to the input frequency divided by $2 \wedge ckPwmRange$.

Port Definitions

ck   input, global clock signal

cmpPwm   input bus, 8-bit reference value which is compared to *cntPwm* (if *cmpPwm* is smaller, then the output *pwm_out* will be LOW, else it will be HIGH)

pwm_out   output, the PWM signal output