

## Overview

This document describes the project used to compile the Basys2 User Demo. The demo configuration is programmed into the Basys2 Platform Flash at the factory.

The User Demo demonstrates basic usage of the Basys2 switches, buttons LEDs, 7-segment display, and VGA connector. The project files can be used as a starting point for simple designs using these components. Although the User Demo can then be used for limited in-field testing, the User Test in the Adept application is recommended for complete testing.

The User Demo configuration file contains behavioral demo components for:

### Input Devices

- 8x switch (SW7, SW6, SW5, SW4, SW3, SW2, SW1, SW0)
- 4x button (BTN3, BTN2, BTN1, BTN0)

### Output Devices

- 8x User LEDs (LD7, LD6, LD5, LD4, LD3, LD2, LD1, LD0)
- four digit seven-segment display (DISP1)

### Connectors

- a VGA display attached to the VGA connector (J2)

## Functional Description

Figure 1 shows the Basys2 User Demo project block diagram. The behavior for each block is described below.

### Port Definitions

#### Clock Signals

mclk	in, MCLK (50MHz from IC5)
uclk	in, UCLK (50MHz from IC6 socket)

#### Seven-Segment Display Signals

seg	out 7-bit, cathode
an	out 4-bit, anode
dp	out, decimal point cathode

### LED, Switch, Button Signals

led	out 7-bit, cathode
sw	in 8-bit, switch input
btn	in 4-bit, button input

### VGA Signals

HSync	out, horizontal sync
VSynC	out, vertical sync
OutRed	out 3-bit, red
OutGreen	out 3-bit, green
OutBlue	out 2-bit, blue

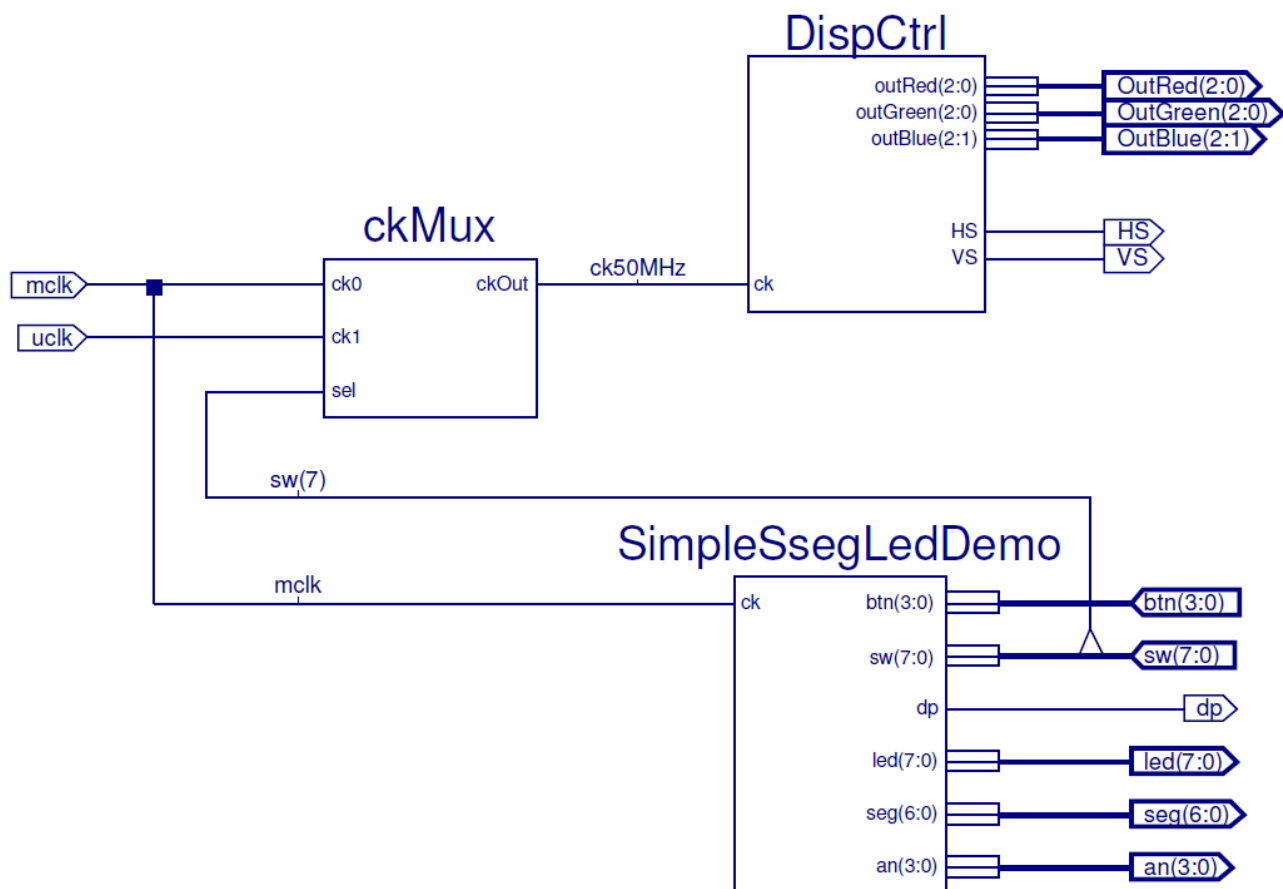


Figure 1 The Basys2 User Demo Project

## ckMux

The ckMux component instantiates a BUFGMUX Xilinx Primitive to select between two possible clock sources for the DispCtrl component: MCLK (when sw(7) = '0') or UCLK (when sw(7) = '1'). Only the VGA demo is affected, the rest of the project always uses MCLK.

## DispCtrl

The Basys2 User Demo project contains the design for a VGA image generator. A horizontal colored-bar pattern is shown on the VGA display (640X480, 60Hz mode).

From the top to the bottom of the screen, there are:

- 8 red bars (increasing intensity, corresponding to all possible values of the 3 bits of OutRed)
- 8 green bars (increasing intensity, corresponding to all possible values of the 3 bits of OutGreen)
- 4 blue bars (increasing intensity, corresponding to all possible values of the 2 bits of OutBlue)
- 4 grey bars (increasing intensity, corresponding to all possible values of the most significant 2 bits of OutRed = OutGreen = OutBlue)
- Same pattern repeats until filling the screen.

When using MCLK (sw(7) = '0'), the image generated by the Basys2 User Demo project is poor quality: vertical edges are folded and wavering. Some LCD displays cannot synchronize the image at all and show black. The reason for that is the unstable frequency generated by the RC oscillator IC5. The MCLK clock signal is good for applications which do not require a very precise and stable frequency, but is not appropriate for more advanced projects (video, asynchronous serial transmissions, etc.)

When using UCLK (sw(7) = '1') with a crystal oscillator loaded into the IC6 socket, the image generated by the Basys2 User Demo project is higher quality, with stable vertical edges.

## SimpleSsegLedDemo

The SimpleSsegLedDemo file contains the demo for the seven-segment display and the LEDs on the Basys2 board.

Each switch controls the state of an LED (SW0 -> LED0, etc.). When the switch is '1' (UPPER position), the corresponding LED is ON, and vice-versa.

A hexadecimal counter is shown on each digit of the seven segment display. All decimal points are ON. Pressing a BTN turns the corresponding digit OFF.